WE CLAIM:

1. A system comprising:

a plurality of functional devices accessing a memory bus wherein said memory bus allows access by one of said functional devices for one cycle of period of time;

a plurality of request agents corresponding to said functional devices;

a control register respectively storing access priority grades for said request agents;

a plurality of counter timers respectively loading said access priority grades; and

a bus elector coupled with said counter timers wherein said bus elector respectively compares said loaded access priority grades and elects one out of said request agents according to said compared access priority grades;

wherein said memory bus allows access by one of said functional devices corresponding to said elected request agent for one cycle of period of time.

2. The system of claim 1 wherein said functional devices are selected from the group consisting of memory controllers, image processors, motion estimation processors, host and peripheral interfaces.

3. The system of claim 1 wherein said access priority grades are counter values ranging from largest to smallest and said elected request agent is one that includes the smallest counter value.

4. The system of claim 1 wherein said access priority grades are counter values ranging from largest to smallest and said elected request agent is one that includes the largest counter value.

5. The system of claim 1 further comprising a control unit for connected to said request agents for respectively receiving corresponding requests for access to said memory bus.

6. A memory bus arbiter for a system having a plurality of functional devices accessing

a memory bus with a plurality of request agents corresponding to the functional devices, the memory bus arbiter comprising:

a control register respectively storing access priority grades for said request agents;

a plurality of counter timers respectively loading said access priority grades; and

a bus elector coupled with said counter timers wherein said bus elector respectively compares said loaded access priority grades and elects one out of said request agents according to said compared access priority grades;

wherein said memory bus allows access by one of said functional devices corresponding to said elected request agent for one cycle of period of time.

7. The memory bus arbiter of claim 6 wherein said functional devices are selected from the group consisting of memory controllers, image processors, motion estimation processors, host and peripheral interfaces..

8. The memory bus arbiter of claim 6 wherein said access priority grades are counter values ranging from largest to smallest and said elected request agent is one that includes the smallest counter value.

9. The memory bus arbiter of claim 6 wherein said access priority grades are counter values ranging from largest to smallest and said elected request agent is one that includes the largest counter value.

10. The memory bus arbiter of claim 6 further comprising a control unit for connected to said request agents for respectively receiving corresponding requests for access to said memory bus.

11. A method for a system having a plurality of functional devices accessing a memory bus, the method comprising the steps of:

(a) providing a plurality of request agents respectively corresponding to said functional devices;

(b) storing access priority grades for said request agents;

(c) comparing said access priority grades;

(d) electing a request agent out of said request agents according to said compared access priority grades; and

(e) allowing access to said memory bus for one cycle of period of time by one of said functional devices corresponding to said elected request agent to said memory bus.

12. The method of claim 11 further comprising the step of repeating steps (c), (d) and (e) for a plurality of cycles of period of time.

13. The method of claim 11 wherein said access priority grades are counter values ranging from largest to smallest and said elected request agent is one that includes the smallest counter value.

14. The method of claim 11 wherein said access priority grades are counter values ranging from largest to smallest and said elected request agent is one that includes the largest counter value.

15. The method of claim 11 wherein said functional devices are selected from the group consisting of memory controllers, image processors, motion estimation processors, host and peripheral interfaces.